CLAIMS

What is claimed is:

1. A method for electrically connecting a semiconductor chip to an array of solder balls on a BGA package; the semiconductor chip having an array of bond pads and being mounted on a substrate;

the method comprising the steps of:

(1) providing a plurality of electrically-conductive bond fingers, each bond finger being electrically connected to the corresponding one of the bond pads on the semiconductor chip;

(2) providing a plurality of electrically conductive vias, each via penetrating through the substrate and electrically connected to one of the solder balls;

(3) providing a plurality of continuous electrically-conductive traces on the substrate for electrically connecting a subgroup of the bond fingers to their corresponding ones of the vias;

(4) if any one of the continuous electrically-conductive traces is interposed between a corresponding pair of bond finger and via, then performing the following substeps of:

(4-1) providing an electrically-conductive bridge to span in an overhead manner across the interposing electrically-conductive trace, and

(4-2) electrically connecting the two ends of the electrically-conductive bridge respectively to the corresponding pair of bond finger and via.

2. The method of claim 1, wherein in said substep (4-1), the electrically-conductive bridge is a bonding wire mounted through wire-bonding technology.

3. The method of claim 2, wherein the bonding wire is a gold wire.

4. The method of claim 1, wherein in said substep (4-1), the electrically-conductive bridge is a chip resistor mounted through SMT technology.

5. The method of claim 4, wherein chip resistor is a zero-resistance chip resistor.

6. A BGA package, which comprises:

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(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate; the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias; these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge which spans in an overhead manner across each interposing trace and having one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

7. The BGA package of claim 6, wherein the electrically-conductive bridge is a bonding wire mounted through wire-bonding technology.

8. The BGA package of claim 7, wherein the bonding wire is a gold wire.

9. The BGA package of claim 6, wherein the electrically-conductive bridge is a chip resistor mounted through SMT technology.

10. The BGA package of claim 9, wherein chip resistor is a zero-resistance chip resistor.

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ADD A2